

CLEAN COPY OF AMENDED SPECIFICATION PARAGRAPHS:

This application is a Divisional of Application Serial No. 09/095,612 filed June 11, 1998 now
Patent No. 6,194,758.

CLEAN COPY OF AMENDED CLAIMS:

12. (Twice Amended) A semiconductor device including a memory cell region and a peripheral circuit region, comprising:

a semiconductor substrate having a major surface;

an insulating film, having an upper surface, being formed on said major surface of said
5 semiconductor substrate to extend from said memory cell region to said peripheral circuit region;

a capacitor lower electrode assembly, including first and second lower electrodes being
adjacent to each other through a part of said insulating film, being formed on said major surface
of said semiconductor substrate to extend up to a vertical position substantially identical to that
of said upper surface of said insulating film in said memory cell region;

10 first and second openings formed in the insulating film, and the first and the second lower
electrodes formed within the first and second openings, respectively;

said first and second lower electrodes each of a cylindrical shape having an interior
region;

wherein respective sidewalls of the first and the second lower electrodes are formed to
15 extend in a longitudinal direction with respect to the major surface of the semiconductor
substrate, each sidewall having a cross-section in the longitudinal direction which is substantially
linear; and

a capacitor upper electrode being formed on said capacitor lower electrode assembly
through a dielectric film to extend onto said upper surface of said insulating film, said upper
20 electrode being formed on the interior region of each of the first and second electrodes,

said capacitor lower electrode assembly including a capacitor lower electrode part
upwardly extending in opposition to said capacitor upper electrode and having a top surface and
a bottom surface.